I hereby certify that this correspondence is being deposited with the united states postal service as in an envelope addressed to: commissioner of patents and trademarks,ALEXANDRIA, VA 22313-1450, on 10/08/03 .
The applicant and/or attorney requests the date of deposit as the filing date. Depositor: KAREN CINQ-MARS

Karen Cinq-Mars 10/8/03
(Signature & date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of :	10/08/03
Bertrand Gabillard :	Group Art Unit:
Serial No. 10/605,361 :	Examiner:
Filed: 9/25/03	International Business Machines Corporation 2070 Route 52 Hopewell Junction, NY 12533

TITLE: AN IMPROVED VOLTAGE TO CURRENT CONVERTER CIRCUIT

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Bertrand Gabillard

By James J. Cioffi
James J. Cioffi Attorney
Registration No. 51,564
Telephone No. 845-894-3363

FR920020014US1

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
FR920020014US1	10/605,361

Applicant(s): BERTRAND GABILLARD

Filing Date	Group Art Unit
9/25/03	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Article: "Fully Integrated CMOS Phase- Locked Loop with 15 to 240 MHz Locking Range and+50 ps Jitter", IEEE JOURNAL OF SOLID-STATE CIRCUITES, VOL. 30, NO.11, NOVEMBER 1995

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.